THAT WHICH IS CLAIMED IS:

1. A microprocessor to be connected to a first memory through a first bus and to a second memory through a second bus, the microprocessor comprising:

a processing unit;

a program access bus connected to said processing unit;

a data access bus connected to said processing unit; and

a bus interface unit connected to the first and second buses, to said program access bus and to said data access bus, said bus interface unit comprising

a first switching circuit for connecting said program access bus to either the first bus or the second bus in accordance with a program access request sent by said processing unit, and

a second switching circuit for connecting said data access bus to either the first bus or the second bus in accordance with a data access request sent by said processing unit.

2. A microprocessor according to Claim 1, wherein said first switching circuit is independent of said second switching circuit; and wherein said bus interface unit further comprises an access control circuit for arbitrating accessing contention occurring when said processing unit simultaneously sends the data access request and the program access request relating to a same memory space.

3. A microprocessor according to Claim 2, wherein said access control circuit grants priority to the data access request when contention for accessing

the first memory and the second memory occurs.

4. A microprocessor according to Claim 2, wherein said access control circuit grants concurrent access to a program instruction within one of the first and second memories and a data element within the other of the first and second memories.

5. A microprocessor according to Claim 2, wherein said access control circuit prevents said processing unit from accessing a program instruction due to said processing unit sending concurrent requests for accessing the program instruction and a data element in a same memory space.

6. A microprocessor according to Claim 2, wherein said access control circuit grants said processing unit access to either the first memory or the second memory for a time period during which each memory grants access thereto.

7. A microprocessor according to Claim 6, wherein said processing unit is connected to a program instruction address decoder and a data address decoder; the program instruction address decoder and the data address decoder generating a plurality of selection signals in accordance with addresses present on said program access bus and said data access bus and in accordance with the program access request sent by said processing unit, the plurality of selection signals including two selection signals for indicating a request for accessing a program instruction in the first and second memories, respectively, and two more selection signals for indicating a request for accessing a data element in the first and second memories, respectively.

8. A microprocessor according to Claim 7, wherein said first switching circuit connects said program access bus to the first bus or the second bus when the plurality of selection signals indicate a request for accessing the program instruction in the first or second memory, and does not indicate a concurrent request for accessing the data element therein.

9. A microprocessor according to Claims 7, wherein said second switching circuit connects said data access bus to the first bus or the second bus when the plurality of selection signals indicate a request for accessing the data element in the first or second memory.

10. A microprocessor according to Claim 1, wherein the first memory comprises a non-volatile memory and the second memory comprises a volatile memory.

11. A microprocessor to be connected to a first memory through a first bus and to a second memory through a second bus, the microprocessor comprising:

a processing unit;

a program access bus connected to said processing unit;

a bus interface unit connected to the first and second buses, to said program instruction access bus and to said data access bus, said bus interface unit comprising

a first switching circuit for connecting said program access bus to either the first bus or the second bus in accordance with a program access request sent by said processing unit, and

a second switching circuit for

connecting said data access bus to either the first bus or the second bus in accordance with a data access request sent by said processing unit; and

an access control circuit for arbitrating accessing contention occurring when said processing unit simultaneously sends the data access request and the program access request relating to a same memory space.

12. A microprocessor according to Claim 11, wherein said first switching circuit is independent of said second switching circuit.

13. A microprocessor according to Claim 11, wherein said access control circuit grants priority to the data access request when contention for accessing the first memory and the second memory occurs.

14. A microprocessor according to Claim 11, wherein said access control circuit grants concurrent access to a program instruction within one of the first and second memories and a data element within the other of the first and second memories.

15. A microprocessor according to Claim 11, wherein said access control circuit prevents said processing unit from accessing a program instruction due to said processing unit sending concurrent requests for accessing the program instruction and a data element in a same memory space.

16. A microprocessor according to Claim 11, wherein said access control circuit grants said processing unit access to either the first memory or the second memory for a time period during which each memory grants access thereto.

17. A microprocessor according to Claim 11, wherein the first memory comprises a non-volatile memory and the second memory comprises a volatile memory.

18. A microprocessor system comprising:

a first memory and a first bus connected thereto;

a second memory and a second bus connected thereto; and

a microprocessor connected to said first and second memories via said first and second buses, respectively, said microprocessor comprising

a processing unit,

a program access bus connected to said processing unit,

a data access bus connected to said processing unit, and

a bus interface unit connected to said first and second buses, to said program access bus and to said data access bus, said bus interface unit comprising

a first switching circuit for connecting said program access bus to either the first bus or the second bus in accordance with a program access request sent by said processing unit, and

a second switching circuit for connecting said data access bus to either the first bus or the second bus in accordance with a data access request sent by said processing unit.

19. A microprocessor system according to Claim 18, wherein said first switching circuit is

independent of said second switching circuit; and wherein said bus interface unit further comprises an access control circuit for arbitrating accessing contention occurring when said processing unit simultaneously sends the data access request and the program access request relating to a same memory space.

20. A microprocessor system according to Claim 19, wherein said access control circuit grants priority to the data access request when contention for accessing said first memory and said second memory occurs.

21. A microprocessor system according to Claim 19, wherein said access control circuit grants concurrent access to a program instruction within one of said first and second memories and a data element within the other of said first and second memories.

22. A microprocessor system according to Claim 19, wherein said access control circuit prevents said processing unit from accessing a program instruction due to said processing unit sending concurrent requests for accessing the program instruction and a data element in a same memory space.

23. A microprocessor system according to Claim 19, wherein said access control circuit grants said processing unit access to either said first memory or said second memory for a time period during which each memory grants access thereto.

24. A microprocessor system according to Claim 23, further comprising:

a program instruction address decoder connected to said microprocessor; and

a data address decoder connected to said microprocessor;

said program instruction address decoder and said data address decoder for generating a plurality of selection signals in accordance with addresses present on said program access bus and said data access bus and in accordance with the program access request sent by said processing unit, the plurality of selection signals including two selection signals for indicating a request for accessing a program instruction in said first and second memories, respectively, and two more selection signals for indicating a request for accessing a data element in said first and second memories, respectively.

25. A microprocessor system according to Claim 18, wherein said first memory comprises a non-volatile memory and said second memory comprises a volatile memory.

26. A method for accessing an instruction code stored in a first memory and a data element stored in a second memory using a microprocessor, with the first and second memories being connected to the microprocessor via first and second buses, respectively, and the microprocessor comprises an executable program instruction access bus connected to a processing unit, a data access bus connected to the processing unit, and a bus interface unit connected to the first and second buses, to the program access bus and to the data access bus, the method comprising:

connecting the program access bus to either the first bus or the second bus in accordance with a program access request sent by the processing unit; and

connecting the data access bus to either the first bus or the second bus in accordance with a data access request sent by the processing unit.

27. A method according to Claim 26, wherein the first switching circuit is independent of the second switching circuit; and further comprising arbitrating accessing contention occurring when the processing unit simultaneously sends the data access request and the program access request relating to a same memory space.

28. A method according to Claim 27, wherein arbitrating accessing contention further comprises preventing the processing unit from accessing a program instruction due to the processing unit sending concurrent requests for accessing the program instruction and a data element in a same memory space.

29. A method according to Claim 27, wherein arbitrating accessing contention further comprises granting the processing unit access to either the first memory or the second memory for a time period during which each memory grants access thereto.

30. A method according to Claim 29, wherein the processing unit is connected to a program instruction address decoder and to a data address decoder, the program instruction address decoder and the data address decoder generating a plurality of selection signals in accordance with addresses present on the program access bus and the data access bus and in accordance with the program access request sent by the processing unit, the plurality of selection signals including two selection signals for indicating a request for accessing a program instruction in the first and second memories, respectively, and two more selection signals for indicating a request for accessing a data element in the first and second memories, respectively.

31. A method according to Claim 30, further comprising connecting the program access bus to the first bus or the second bus when the plurality of selection signals indicate a request for accessing the program instruction in the first or second memory, and does not indicate a concurrent request for accessing the data element therein.

32. A method according to Claim 30, further comprising connecting the data access bus to the first bus or the second bus when the plurality of selection signals indicate a request for accessing the data element in the first or second memory.

33. A method according to Claim 26, wherein the first memory comprises a non-volatile memory and the second memory comprises a volatile memory.